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(54) **Serial bus control apparatus**

(57) Conventional serial bus of IEEE 1394 can not manage a transmission bandwidth and transmission channel for a future time. Therefore, it is not possible to make a reservation for recording from a STB to a VCR connected to the bus. The present invention makes it possible to perform a reservation management of the bus by defining and utilizing registers on CSR space for managing reservations of transmission bandwidth and transmission channel from present time to a future time.

In order to achieve the objects, a serial bus control apparatus of the present invention includes a means for providing a table for controlling a serial bus which has a function for securing a transmission bandwidth for the packet to the serial bus. The table is a reservation control table at least indicating a reservation of a transmission bandwidth and a transmission channel which is required from time T1 until time T2, the reservation control table is stored and controlled on a first register assigned to an address space which is accessible for reading and writing from an arbitrary node on the serial bus. The serial bus control apparatus of the present invention preferably includes a first detection part to detect that the present time is the time T1, the time T2, or the time between T1 and T2. Moreover, the serial bus control apparatus of the present invention preferably includes a rewriting part for rewriting a second register and a third register assigned to a particular address space for a particular node on the serial bus, which second register indicates the available transmission bandwidth at present time and which third register indicates the utilization status of the transmission channel at present time. The particular node on the serial bus is a node, which belongs to the serial bus control apparatus,

and a node which includes the second register and the third register control apparatus of the present invention. The serial bus control apparatus of the present invention preferably includes a register providing part for providing a register for reservation control table which table is accessible for reading and writing from an arbitrary node of an arbitrary bus of the N piece of serial buses having the same standard time. In accordance with the present invention, a reservation management for future time using a serial bus for securing the transmission bandwidth and transmission channel according to IEEE 1394 can be achieved, which is not possible with conventional technology. Moreover the serial bus control apparatus of this invention is compatible with conventional systems.

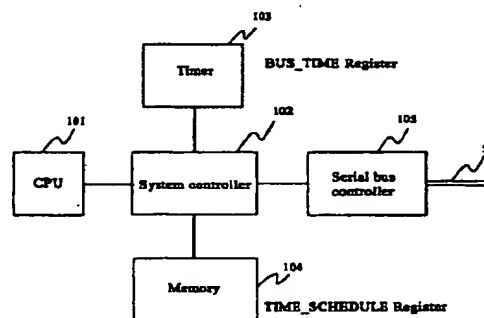


Fig. 1

**[0006]** Figure 11 and Figure 12 show the bit allotment

**[0008]** In order to perform the isochronous transmission, the transmission bandwidth (corresponding to 125  $\mu$ sec) and the transmission channel are secured by setting of the BANDWIDTH\_AVAILABLE register and the CHANNELS\_AVAILABLE register, then the cycle start packet is transmitted as shown in Figure 13(a), afterward the isochronous packet is transmitted after a gap time which is called an isochronous gap. In Figure 13(a), 12 indicates the period which is called a bus arbitration period, two or more nodes request the packet transmission to one bus at the same time, only one node can acquire the authority for the packet transmission. 13 indicates a period which is called a data prefix

period, or the period after which the packet is immediately transmitted. 14 indicates isochronous packet period, or the period for which the transmission data is transmitted. 15 indicates a period which is called the data end, it indicates that the transmission of the packet is ended. As shown in Figure 13(b), the period in which the isochronous packet can be transmitted is about 100  $\mu$ sec after the cycle start, or the period for which the packet of two or more channels can be transmitted.

[0009] As shown in Figure 10, in this case, the second digital VCR is an IRM, the BANDWIDTH\_AVAILABLE register and the CHANNELS\_AVAILABLE register are available to IEEE 1394 serial bus 5. When the digital data of the first digital VCR is transmitted to the second digital VCR using the isochronous transmission, the data transmission (dubbing) is started after securing the transmission bandwidth and the transmission channel by the above-mentioned procedure. For instance, the first digital VCR and the second digital VCR are equipped with a physical layer which has the transmission ability of S100 (it is the transmission standard of 98.304 Mbps in the IEEE 1394). When the bandwidth of 40Mbps is transmitted by the channel 0, 40Mbps corresponds to 2500d, isochronous transmission is started with rewriting the value of bw\_remaining as 0100101101111 (because  $4915d - 2500d = 2415d = 0100101101111$ ), and the 0th bit of the channels\_available\_lo as 0b.

[0010] However, the above mentioned conventional serial bus control apparatus can only secure the current transmission bandwidth and the current transmission channel. There is no concept for time reservation of the transmission bandwidth and transmission channel. Therefore, when it is necessary to use the bus at certain period in future, it is not sure that the required transmission bandwidth and transmission channel is available or not.

[0011] Because of this, there are inconveniences in the serial bus control apparatus. For instance, when recording a program from the set top box connected with the bus to the digital VCR at certain time in the future with reservation by the timer, and if other nodes occupied the bus at the reserved time, the reserved recording by the timer can not be performed.

[0012] Therefore, with the foregoing in mind, it is an object of the present invention to provide a serial bus control apparatus for controlling the utilization of a bus, which can secure a transmission bandwidth and a channel of IEEE 1394 serial bus, at present time and future time.

[0013] In order to achieve the objects, a serial bus control apparatus of the present invention includes a means for providing a table for controlling a serial bus which has a function for securing a transmission bandwidth for the packet to the serial bus. The table is a reservation control table at least indicating a reservation of a transmission bandwidth and a transmission channel which is required from time T1 until time T2, the reser-

vation control table is stored and controlled on a first register assigned to an address space which is accessible for reading and writing from an arbitrary node on the serial bus.

[0014] In one embodiment, the serial bus control apparatus of the present invention preferably includes a first detection part to detect that the present time is the time T1, the time T2, or the time between T1 and T2. Moreover, the serial bus control apparatus of the present invention preferably includes a rewriting part for rewriting a second register and a third register assigned to a particular address space for a particular node on the serial bus, which second register indicates the available transmission bandwidth at the present time and which third register indicates the utilization status of the transmission channel at the present time.

[0015] In one embodiment, the particular node on the serial bus is a node, which belongs to the serial bus control apparatus, and a node which includes the second register and the third register control apparatus of the present invention preferably includes the second and third registers.

[0016] In one embodiment, the serial bus control apparatus of the present invention preferably includes a register providing part for providing a register for reservation control table which table is accessible for reading and writing from an arbitrary node of an arbitrary bus of the N piece of serial buses having the same standard time.

[0017] In accordance with the present invention, A reservation management for future time using a serial bus for securing the transmission bandwidth and transmission channel according to IEEE 1394 can be achieved, which is not possible with conventional technology. Moreover, the serial bus control apparatus of this invention is compatible with conventional systems.

[0018] These and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

Figure 1 is a block diagram showing a serial bus control apparatus of Embodiment 1 of this invention.

Figure 2 is a first bit field chart showing a TIME\_SCHEDULE register of this invention.

Figure 3 is a bus block diagram of Embodiment 1 of this invention.

Figure 4 (a) is a reservation table of Embodiment 1 of this invention.

Figure 4 (b) is a bit field chart showing TIME\_SCHEDULE register of Embodiment 1 of this invention.

Figure 5 is a register state transition diagram of Embodiment 1 of this invention.

Figure 6 is a block diagram showing a serial bus control apparatus of Embodiment 2 of this invention.

Figure 7 is a bus block diagram of Embodiment 2 of this invention.

Figure 8 (a) is a reservation table of Embodiment 2 of this invention.

Figure 8 (b) to (d) are bit field charts showing 5  
TIME\_SCHEDULE registers of Embodiment 1 of this invention.

Figure 9 is a register state transition diagram of Embodiment 2 of this invention.

Figure 10 is a bus block diagram of the conventional 10  
technology.

Figure 11 is a bit field chart of showing BANDWIDTH\_AVAILABLE register of IEEE 1394.

Figure 12 is a bit field chart of showing CHANNELS\_AVAILABLE register of IEEE 1394. 15

Figure 13 (a) and (b) are a status charts showing an isochronous transmission of IEEE 1394.

Figure 14 is a bit field chart showing a BUS\_TIME register of IEEE 1394.

Figure 15 is a second bit field chart showing a 20  
TIME\_SCHEDULE register of this invention.

[0019] Hereinafter, the present invention will be described by way of embodiments with reference to the accompanying drawings.

(Embodiment 1)

[0020] Figure 1 shows a block diagram of a node which includes a first preferred example of a serial bus control apparatus of this invention.

[0021] In Figure 1, 101 denotes a CPU which controls a node. 102 denotes a system controller which includes an interface for the CPU 101, a memory 104, a timer 103 and a serial bus controller 105. 105 denotes a serial bus controller 105 for controlling data transmission of a serial bus of IEEE 1394. 5 denotes a serial bus of IEEE 1394. By this composition, a register which is called a TIME\_SCHEDULE register is provided to the IEEE serial bus. The serial bus control apparatus of this invention is called as a Time Schedule Manager (hereinafter, referred to as TSM). The TSM composed as mentioned above can be built into personal computer 3 of Figure 3 for instance.

[0022] Figure 3 shows the bus composition which includes the node which has a serial bus controller (Time Schedule Manager, hereinafter referred to as TSM), of this invention.

[0023] 1 denotes a first digital VCR, 2 denotes a second digital VCR, 3 denotes a personal computer, 4 denotes a set top box (hereinafter, referred to as STB). It is assumed that the transmission ability of the physical layer is S100.

[0024] Physical\_ID is allotted to each node based on the rule of IEEE1394. The physical\_ID allotted to the first digital VCR 1 is 3 (physical\_ID = 3), the physical\_ID allotted to the second digital VCR 2 is 1 (physical\_ID = 1), the physical\_ID allotted to the personal computer 3

is 0 (physical\_ID = 0), the physical\_ID allotted to the first set top box 4 is 2 (physical\_ID = 2).

[0025] In this example, the first digital VCR of physical\_ID=3 performs as an IRM, and provides the BANDWIDTH\_AVAILABLE register and the CHANNELS\_AVAILABLE register to the IEEE 1394 serial bus. This node includes a CM function and performs the broadcast of the cycle start packet to the bus.

[0026] The TIME\_SCHEDULE register is provided to the CSR space of the personal computer 3. The substance of the TIME\_SCHEDULE register is the memory 104 shown in Figure 1. If there is a request for writing data to TIME\_SCHEDULE register or reading data from the TIME\_SCHEDULE register by the serial bus controller 105, the CPU 101 actually writes data to memory 104 or reads data from memory 104 and returns the result to the serial bus controller 105.

[0027] Figure 2 shows an example of the bit allotment of the TIME\_SCHEDULE register. The register of three quadlet is defined corresponding to one time schedules. The # 0 to the # M TIME\_SCHEDULE register (M is an integer of 0 or more) is defined in the continuous address to control two or more time schedule.

[0028] In the TIME\_SCHEDULE register, the upper seven bits of the quadlet are not used. The following six bits are physical\_ID of the node which preserves the time schedule. The following six bits indicate the channel number which is reserved and performed with request\_channel\_number. The following 13 bits indicate the bandwidth to be reserved by request\_bw. 30

[0029] The second quadlet indicates the time when the reservation is started and performed. According to the definition of the BUS\_TIME register of IEEE 1394, the upper 25 bits are defined as the start\_second\_count\_hi and the lower 7 bits are defined as start\_second\_count\_lo. 35

[0030] The third quadlet indicates the time when the reservation is ended and performed. According to the definition of the BUS\_TIME register of IEEE 1394, the upper 25 bits are defined as the start\_second\_count\_hi and the lower 7 bits are defined as start\_second\_count\_lo. 40

[0031] Figure 14 shows the BUS\_TIME register of the serial bus of IEEE 1394. It is a counter of 32 bits which counts by second and can count 136 years of time. In the above description, the 32 bits are separated into second\_count\_hi and second\_count\_lo. However, the separation has no special meaning in this Embodiment 1.

[0032] The initial value of the TIME\_SCHEDULE register is request\_bw = 000000000000b. Other bits can take any value. As a result, The ID number of the TIME\_SCHEDULE register which is used for the time reservation can be detected. 50

[0033] As shown in Figure 4 (a), in order to operate the reserved recording from the first set top box shown in Figure 3 to the first digital VCR from 6 o'clock to 18 o'clock on October 10, when the personal computer

reserves 25 Mbps bandwidth by channel 1, the bit assignment are that

```
physical_ID = 000000b,
request_channel_number = 000001b,
request_bw = 0011000100000b,
start_second_count_hi =
0000000000000000010101000b,
start_second_count_lo = 1100000b,
end_second_count_hi =
00000000000000000111111010b,
start_second_count_lo = 0100000b.
```

[0034] This value is written in the TIME\_SCHEDULE register. To simplify explanation, in the BUS\_TIME, 0 o'clock of October 10 is set to as 0.

[0035] Moreover, this reservation is set to the # 0 TIME\_SCHEDULE register and assigned bit in other register is request\_bw=0000000000000b. Therefore, other time reservation is not set.

[0036] Moreover, before reservation, the node performing reservation reads out all TIME\_SCHEDULE registers and confirms that necessary bandwidth and channel are available or not at the time to be reserved. If necessary bandwidth and channel are available at the time to be reserved, the reserved recording can be set.

[0037] Figure 5 shows the change in the BANDWIDTH\_AVAILABLE register and the CHANNELS\_AVAILABLE register of IRM of the reservation mentioned above.

[0038] The values of these registers for between 0 o'clock and 6 o'clock on October 10 are the initial values. In this Embodiment 1, the channels\_available\_hi which is the upper 32 bits of the CHANNELS\_AVAILABLE register is not described because it has not been changed from the initial value. The bandwidth of 25Mbps is used by channel 1 for between 6 o'clock and 18 o'clock on October 10, the isochronous transmission is started with rewriting the bw\_remaining as (1001100110011b - 0011000100000b =>) 01101000110011b, and the channels\_available\_lo as 1111111111111111111111111111101b. Rewriting of these two registers can be performed by any node on the bus. It is not necessary that the node of physical\_ID = 000000b performs the rewriting.

[0039] After 18 o'clock on October 10, the bus is used. Therefore, the BANDWIDTH\_AVAILABLE register and the CHANNELS\_AVAILABLE register are returned to the initial value. When the reserved time is over, request\_bw of the corresponding TIME\_SCHEDULE register should be reserved to 0000000000000b.

[0040] According to the above mentioned preferred Embodiment 1, the serial bus control apparatus of this invention includes a BANDWIDTH\_AVAILABLE register and a CHANNELS\_AVAILABLE register controlled by the IRM as well as TIME\_SCHEDULE register of the TSM of the present invention. The serial bus control apparatus controls the reservation information regard-

ing time schedule by the TIME\_SCHEDULE register and secures the isochronous bandwidth and isochronous channel using the BANDWIDTH\_AVAILABLE register and the CHANNELS\_AVAILABLE register at the time to be reserved.

[0041] According to this operation, the reservation management for future time can be achieved, which is not possible by the conventional technology. Moreover, the serial bus control apparatus of this invention is compatible with conventional systems.

(Embodiment 2)

[0042] Hereinafter, Embodiment 2 of the present invention will be described with reference to the accompanying drawings.

[0043] Figure 6 shows a block diagram of a serial bus bridge as a serial bus control apparatus including plural of serial buses having the TSM of Embodiment 2 of this invention. In Figure 6, 101 denotes CPU, which controls a node. 102 denotes a system controller which includes an interface for the CPU 101, a memory 104, a timer 103 and a serial bus controller 105, 106 and 107. Each 105 to 107 denotes a serial bus controller for controlling data transmission of a serial bus of IEEE 1394. 5 denotes a serial bus of IEEE 1394. By this composition, a register which is called a TIME\_SCHEDULE register is provided to the IEEE serial bus. Normally, it is better that the bus bridge acts as IRM for each bus. Therefore, the BANDWIDTH\_AVAILABLE register and the CHANNELS\_AVAILABLE register to be provided to each bus are equipped. Two or more buses are connected and perform using the above described bus bridge in which TMS is equipped.

[0044] Figure 7 shows the bus composition which includes the plural bus connected via bus bridge having the serial bus controller (TSM) of this invention. 1 denotes a first digital VCR, 2 denotes a second digital VCR, 3 denotes a personal computer, 7 denotes a first digital television set (hereinafter, referred to as TV). These nodes are connected to the serial bus whose BUS\_ID is 0 (BUS\_ID = 0), and connected to the bus bridge 10. 6 denotes a third digital VCR and 4 denotes a first STB. These nodes are connected to the serial bus whose BUS\_ID is 1 (BUS\_ID = 1), and connected to the bus bridge 10. 8 denotes a second STB, and 9 denotes a printer. These nodes are connected to the serial bus whose BUS\_ID is 2, and connected with bus bridge 10. It is assumed that the transmission ability of the physical layer of each bus is S100.

[0045] Physical\_ID is allotted to each node of buses based on the rule of IEEE1394. Regarding the BUS\_ID = 0, the physical\_ID allotted to the first digital VCR 1 is 3 (physical\_ID = 3), the physical\_ID allotted to the second digital VCR 2 is 1 (physical\_ID = 1), the physical\_ID allotted to the personal computer 3 is 0 (physical\_ID = 0), the physical\_ID allotted to the bus bridge 10 is 4 (physical\_ID = 4). Regarding the BUS\_ID = 1, the

physical\_ID allotted to the third digital VC 1 is 1 (physical\_ID = 1), the physical\_ID allotted to the first STB 4 is 0 (physical\_ID = 0), the physical\_ID allotted to the bus bridge 10 is 2 (physical\_ID = 2). Regarding the BUS\_ID = 2, the physical\_ID allotted to the second STB 8 is 1 (physical\_ID = 1), the physical\_ID allotted to the printer 9 is 0 (physical\_ID = 0), the physical\_ID allotted to the bus bridge 10 is 2 (physical\_ID = 2).

[0046] In this example, the bus bridge 10 becomes CM, IRM, and TSM in order to achieve the cycle synchronization of each bus and to control the plural buses efficiently. That is, synchronization is taken respectively for each bus, the cycle start packet is broadcasted, and the independent BANDWIDTH\_AVAILABLE register, CHANNELS\_AVAILABLE register and TIME\_SCHEDULE register are provided to each bus. The substance of each register provided to each bus is a memory 104 shown in Figure 6. If there is a request for writing data to each register or reading data from each register by the serial bus controller 105 ~ 107, the CPU 101 actually writes data to memory 104 or reads data from memory 104 and returns the result to the serial bus controller 105 ~ 107.

[0047] An example of the bit allotment for each register can be the same as Embodiment 1.

[0048] As shown in Figure 8 (a), in order to operate the reserved recording from the first set top box shown in Figure 6 to the third digital VCR from 6 o'clock to 18 o'clock on October 10, when the first STB reserves 25 Mbps bandwidth by channel 0, data transmission is performed on the bus whose BUS\_ID is 0 (BUS\_ID = 0), data is written in the TIME\_SCHEDULE register of the TSM # 1 of the BUS\_ID = 1.

[0049] In this case, as shown in Figure 8 (c) #0, the bit assignments are that

```
physical_ID = 000000b,
request_channel_number = 000000b,
request_bw = 0011000100000b,
start_second_count_hi = 00000000000000010101000b,
start_second_count_lo = 1100000b,

end_second_count_hi=00000000000000001111
1010b,
start_second_count_lo = 0100000b.
```

These values are written in the TIME\_SCHEDULE register of TSM #1. The same as Embodiment 1, to simplify the explanation, in the BUS\_TIME, 0 o'clock of October 10 is set to 0.

[0050] Next, According to Figure 8(a), the recording reservation is performed from the second STB shown in Figure 6 to the first digital VCR from 12 o'clock to 24 o'clock on October 10. The second STB is a node of the bus whose BUS\_ID = 2, and the first digital VCR is a node of the bus whose BUS\_ID = 0. Therefore, data is transmitted over two buses. Therefore, data is written in

the TIME\_SCHEDULE register of each TMS of BUS\_ID=2 and BUS\_ID=0. In this case, reservation to each bus with transmission bandwidth 50Mbps and channel 0 is set.

[0051] It is possible to set reservation using channel 0 of the bus whose BUS\_ID=0 and BUS\_ID=2 which are available from 12 o'clock to 18 o'clock though the channel 0 of the bus whose BUS\_ID=1 has already been used. In this case, data are written in # 0 of the table (d) and # 0 of the table (d) shown in Figure 8.

[0052] When the second STB makes the reservation, the value of the TIME\_SCHEDULE register of the TSM # 2 will be rewritten in order to reserve the bus whose BUS\_ID is 2. The bit assignments are that

```
physical_ID = 000001b,
request_channel_number=000000b,
request_bw=0110001000000b,

start_second_count_hi=00000000000000010101
0001b,
start_second_count_lo=1000000b,

end_second_count_hi=000000000000000101010
0011b,
start_second_count_lo=0000000b.
```

[0053] The value of the TIME\_SCHEDULE register of the TSM # 0 will be rewritten in order to reserve the bus whose BUS\_ID is 0. The bit assignments are that

```
physical_ID = 000100b,
request_channel_number = 000000,
request_bw = 0110001000000b,
start_second-count_hi = 000000000000000101010001b,
start_second_count_lo = 1000000b,
end_second_count_hi = 0000000000000001010100011b,
start_second_count_lo = 0000000b.
```

[0054] In this case, because the node of another bus has made reservation to TSM #0 through the bridge, the physical\_ID of the bridge of BUS\_ID=0 is written to the bit field for physical\_ID. In this case, physical\_ID=000100b.

[0055] In addition, according to Figure 8(a), the recording reservation from the first STB shown in Figure 6 to the second digital VCR is performed from 12 o'clock October 10 to 6 o'clock October 11. In this case, data are transmitted over the bus of which BUS\_ID=1 and the bus of which BUS\_ID = 0. Because channel 0 has already been reserved by both bus whose BUS\_ID=1 and bus whose BUS\_ID=0, it is necessary to reserve other channels. In the above description, channel 1 is selected as a reserved channel because channel 1 in both the bus whose BUS\_ID=0 and the bus whose BUS\_ID=1 is available, another channel can be

selected if it is available in both buses.

[0056] In this case, # 1 in Figure 8(c) and # 1 in Figure 8(b) are selected for writing. The register for the TIME\_SCHEDULE register can be selected from unused available registers (register whose request\_bw = 000000000000b). In the above description, register # 1 is selected.

[0057] When the first STB makes the reservation, the value of the TIME\_SCHEDULE register of the TSM # 1 will be rewritten in order to reserve the bus whose BUS\_ID is 1. The bit assignments are that

```
physical_ID = 000000b,
request_channel_number = 000001b,
request_bw=0000010111100b,
start_second_count_hi
000000000000000101010001b,
start_second_count_lo = 1000000b,
end_second_count_hi
000000000000001101001011b,
start_second_count_lo = 1100000b.
```

[0058] The value of the TIME\_SCHEDULE register of the TSM # 0 will be rewritten in order to reserve the bus whose BUS\_ID = 0. The bit assignments are that

```
physical_ID = 000100b,
request_channel_number = 000001b,
request_bw = 0000010111100b,
start_second_count_hi
000000000000000101010001b,
start_second_count_lo = 1000000b,
end_second_count_hi
000000000000001101001011b,
start_second_count_lo = 1100000b.
```

[0059] In this case, because the node of another bus has made reservation to TSM #0 through the bridge, the physical\_ID of the bridge of BUS\_ID=0 is written to the bit field for physical\_ID. In this case, physical\_ID=000100b.

[0060] The same as Embodiment 1, when a node makes reservation, the node reads out values of all TIME\_SCHEDULE register of buses for reserving the bandwidth and confirms whether the necessary bandwidth and necessary channel remains or not. When the necessary bandwidth and necessary channel remains, the node can make reservation. Thus, three kinds of reservations shown in Figure 8(a) are performed completely.

[0061] Figure 9 shows the change in the BANDWIDTH\_AVAILABLE register and the CHANNELS\_AVAILABLE register of IRM #0 to #2 by the above mentioned reservation. The value of these registers between from 0 o'clock to 6 o'clock on October 10 remains as the initial values. In this Embodiment 2, because the channels\_available\_hi which is the upper 32 bits of the CHANNELS\_AVAILABLE register has not

been changed and remains as initial value, it is not described.

[0062] In the bus whose BUS\_ID = 1, the bandwidth of 25Mbps is used by channel 0 between from 6 o'clock to 18 o'clock on October 10, the isochronous transmission is started with rewriting the bw\_remaining as

```
(1001100110011b - 0011000100000b =)
01101000110011b, and
the channels_available_lo as
1111111111111111111111111111110b.
```

Rewriting of this two register can be performed by any node on the bus. It is not necessary that the node of physical\_ID = 000000b performs the rewriting. Moreover, because the bus bridge is a node which has both the function of TSM and IRM, the node can perform register bit field rewriting automatically by detecting the reserved time arrival by CPU 101 with the built in clock 103.

[0063] Between from 12 o'clock to 18 o'clock on October 10, in order to use 50Mbps bandwidth by channel 0 between the bus whose BUS\_ID = 2 and the bus whose BUS\_ID = 0, and to use 3Mbps bandwidth by channel 1 between the bus whose BUS\_ID = 1 and the bus whose BUS\_ID = 0, the isochronous transmission is started with rewriting the register of the IRM #0 as

```
bw_remaining = 1001100110011b-
0110001000000b-0000010111100b =
0011000110111b,
channels_available_lo =
11111111111111111111111111111100b,
rewriting the register of the IRM #1 as
bw_remaining = 0110100010011b-
0000010111100b = 011000101011b,
channels_available_lo =
11111111111111111111111111111100b,
rewriting the register of the IRM #2 as
bw_remaining = 1001100110011b-
0110001000000b = 0011011110011b,
channels_available_lo =
1111111111111111111111111111110b.
```

Rewriting of these registers can be performed by any node on the bus. It is not necessary that the node which had made reservation performs the rewriting. Moreover, because the bus bridge is a node which has both the function of TSM and IRM, the node can perform register bit field rewriting automatically by detecting the reserved time arrival by CPU 101 with the built in clock 103.

[0064] Between 18 o'clock to 24 o'clock on October 10, the recording from the first STB to the third digital VCR performed on the bus whose BUS\_ID = 1 is finished. At this time, it is necessary to release channel 0 which was used for 25Mbps bandwidth transmission. Therefore, the bit field of the register of the IRM #1

should be rewritten as

the `bw_remaining` = 011000101011b +  
0011000100000b = 10010011011b,  
`channels_available_lo` = 5  
111111111111111111111111111101b.

Moreover, because the reservation time ended, it is necessary to release the `TIME_SCHEDULE` register of TSM #1. Because this was written in Figure 8(c) #0, the `request_bw` should be rewritten as 000000000000b in order to enable other nodes to use this register. Rewriting of these registers can be performed by any node on the bus. It is not necessary that the node which had made reservation performs the rewriting. Moreover, because the bus bridge is a node which has both the function of TSM and IRM, the node can perform register bit field rewriting automatically by detecting the reserved time arrival by CPU 101 with the built in clock 103.

[0065] Between 0 o'clock to 6 o'clock on October 11, the recording from the second STB to the first digital VCR performed between the bus whose `BUS_ID` = 2 and the bus whose `BUS_ID` = 0 is finished. At this time, it is necessary to release channel 0 which was used for 50Mbps bandwidth transmission. Therefore, the bit field of the IRM #0 should be rewritten as

`bw_remaining` = 00110001011b +  
0110001000000b = 10010011011b,  
`channels_available_lo` =  
111111111111111111111111111101b,  
the bit field of the IRM #2 should be rewritten as the  
`bw_remaining` = 0011011110011b +  
0110001000000b = 10010011001b,  
  
`channels_available_lo` = 11111111111111111111  
111111111b.

Moreover, because the reservation time ended, it is necessary to release the `TIME_SCHEDULE` register of TSM #2 and TSM #0. Because this was written in Figure 8(d) #0 and Figure 8(b) #0, the `request_bw` should be rewritten as 000000000000b in order to enable other nodes to use this register. Rewriting of these registers can be performed by any node on the bus. It is not necessary that the node which had made reservation performs the rewriting. Moreover, because the bus bridge is a node which has both the function of TSM and IRM, the node can perform register bit field rewriting automatically by detecting the reserved time arrival by CPU 101 with the built in clock 103.

[0066] After 6 o'clock on October 11, the recording from the first STB to the second digital VCR performed between the bus whose `BUS_ID` = 1 and the bus whose `BUS_ID` = 0 is finished. At this time, it is necessary to release channel 1 which was used for 3Mbps bandwidth transmission. Therefore, the bit field of the IRM #0

should be rewritten as the `bw_remaining` =  
100100111011b + 0000010111100b =  
100110011001b, `channels_available_lo` =  
11111111111111111111111111111b, the bit field  
of the IRM #1 should be rewritten as

`bw_remaining` = 100100111011b +  
0000010111100b = 100110011001b,  
`channels_available_lo` =  
11111111111111111111111111111b.

Moreover, because the reservation time ended, it is necessary to release the `TIME_SCHEDULE` register of TSM #1 and TSM #0. Because this was written in Figure 8(c) #0 and Figure 8(b) #0, the `request_bw` should be rewritten as 000000000000b in order to enable other nodes to use this register. Rewriting of these registers can be performed by any node on the bus. It is not necessary that the node which had made reservation performs the rewriting. Moreover, because the bus bridge is a node which has both the function of TSM and IRM, the node can perform register bit field rewriting automatically by detecting the reserved time arrival by CPU 101 with the built in clock 103.

[0067] According to the above mentioned preferred Embodiment 2, the serial bus control apparatus of this invention includes `BANDWIDTH_AVAILABLE` registers and `CHANNELS_AVAILABLE` registers controlled by the IRM as well as `TIME_SCHEDULE` register of the TSM of the present invention. The serial bus control apparatus controls the reservation information regarding time schedule by the `TIME_SCHEDULE` register and secures the isochronous bandwidth and isochronous channel using the `BANDWIDTH_AVAILABLE` register and the `CHANNELS_AVAILABLE` register at the time to be reserved.

[0068] According to this operation, the reservation management for future time can be achieved, which is not possible with conventional technology. Moreover, the serial bus control apparatus of this invention is compatible with conventional systems. The `TIME_SCHEDULE` register of this Embodiment does not prepare the bit for describing `BUS_ID` of the node which made reservation, `BUS_ID` can be added as shown in Figure 15 in order to control.

[0069] In the case where a conventional node, which does not correspond to the TSM of the present invention, is connected to the bus of the present invention, there are problems in that the conventional node reserves the transmission bandwidth and the transmission channel for IRM without reservation registration in the `TIME_SCHEDULE` register and starts the isochronous packet transmission. Another problem is that the conventional node releases the transmission bandwidth and the transmission channel for IRM without canceling the reservation for the `TIME_SCHEDULE` register.

[0070] In order to prevent these problems, it is neces-



sary to prohibit the conventional node to access the IRM and TSM. These problems will be solved if the node which corresponds to TSM of this invention performs the reservation and cancellation for bandwidth and channel to IRM and TSM, and the conventional node performs the actual isochronous packet transmission. However, in the case that the conventional node, which does not know the existence of the TSM of the present invention, performs the access for IRM independently and transmits isochronous packet without registration to TSM, for example, in Figure 8(a), the 40 Mbps isochronous transmission from the first conventional node to the second conventional node without registering TSM, it is impossible to start the reserved 50 Mbps transmission from 12 o'clock on October 10 because of available bandwidth overflow. In this case, the operation of the conventional node should be stopped for stopping the 40 Mbps transmission in order to recover the status of the system as the normal status.

[0071] It is also possible to solve the problems by stopping the reserved 50 Mbps transmission from 12 o'clock.

[0072] What measures should be taken for these problems is selected by system application with consideration of the priority and the appropriate countermeasure that should be performed.

[0073] Moreover, the serial bus of IEEE 1394 is used in the above described Embodiment, other buses are acceptable if that can perform transmission by which the transmission bandwidth is secured.

[0074] The invention may be embodied in other forms without departing from the spirit or essential characteristics thereof. The embodiments disclosed in this application are to be considered in all respects as illustrative and not limitative, the scope of the invention is indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

## Claims

### 1. A serial bus control apparatus comprising:

a means for providing a table for controlling a serial bus which has a function for securing a transmission bandwidth for a packet to the serial bus;

wherein the table is a reservation control table at least indicating a reservation of a transmission bandwidth and a transmission channel which is required from time T1 until time T2, the reservation control table is stored and controlled on a first register assigned to an address space which is accessible for reading and writing from an arbitrary node on the serial bus.

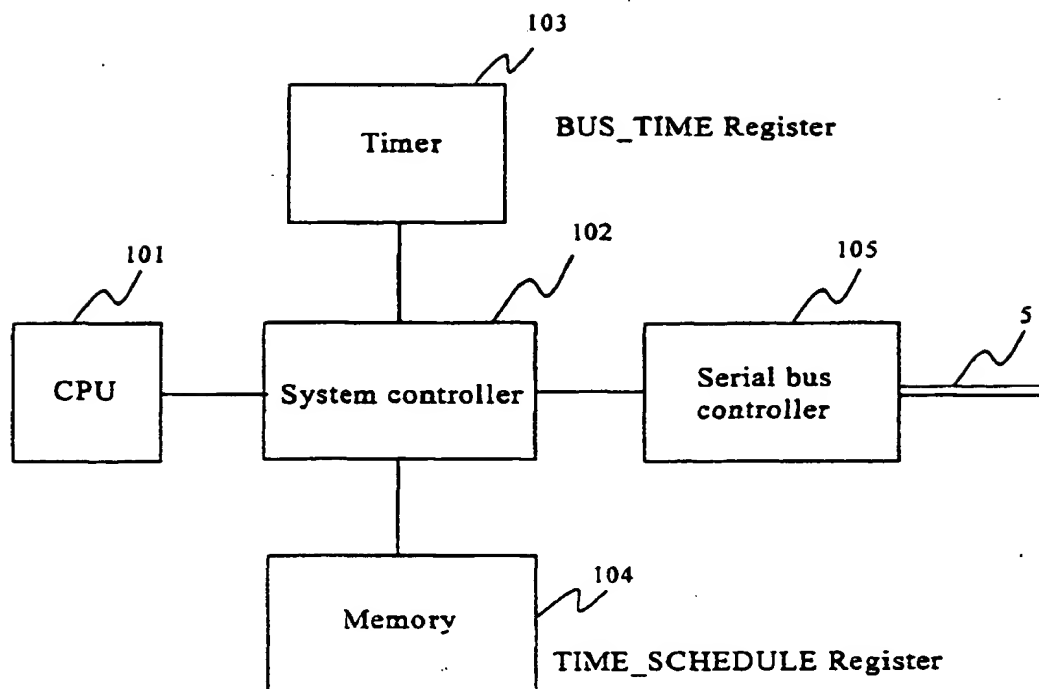
### 2. The serial bus control apparatus according to claim

1, further comprising a first detection part to detect that a present time is the time T1, the time T2, or time between T1 and T2, a rewriting part for rewriting a second register and a third register assigned to a particular address space for a particular node on the serial bus, which second register indicates available transmission bandwidth at present time and which third register indicates utilization status of the transmission channel at present time.

### 3. The serial bus control apparatus according to claim 2 wherein

the particular node on the serial bus is a node, which belongs to the serial bus control apparatus, and a node which includes the second register and the third register.

### 4. The serial bus control apparatus according to any one of claims 1 to 3, further comprising a register providing part for providing a register for reservation control table which table is accessible for reading and writing from an arbitrary node of an arbitrary bus of an N piece of serial buses having a same standard time.



*Fig. 1*

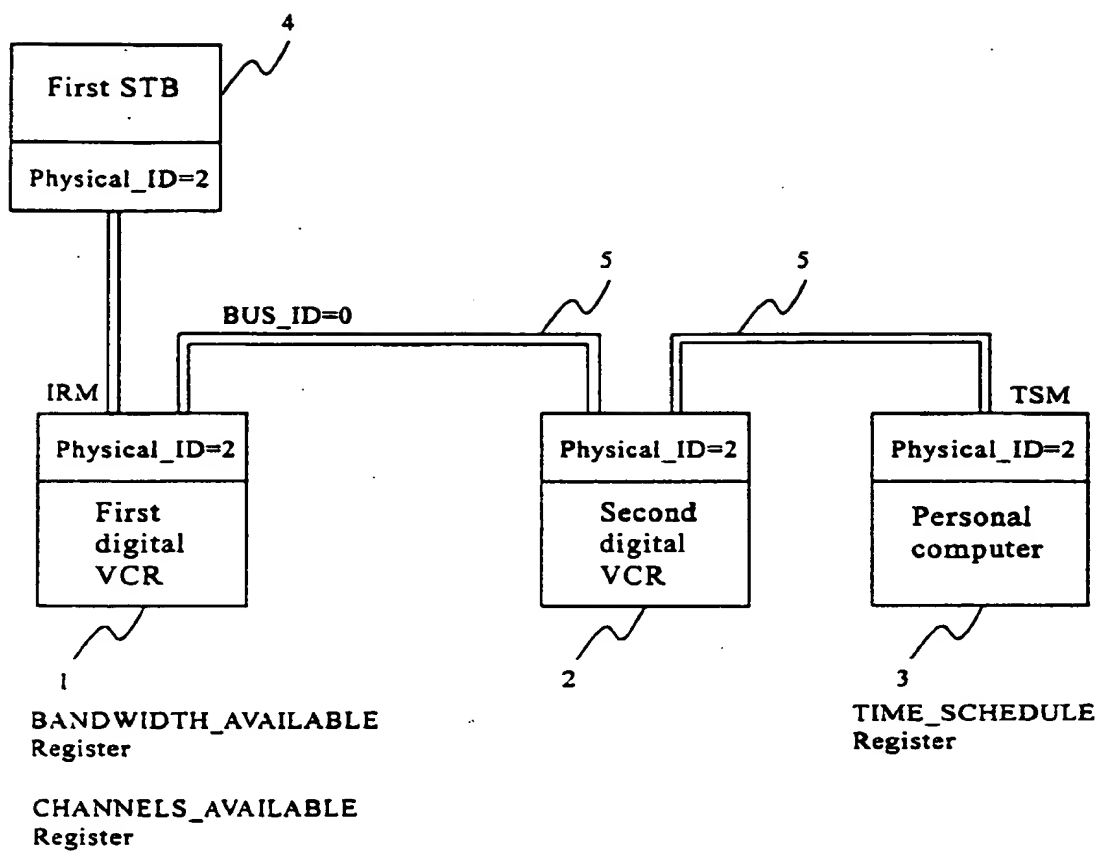
## Definition

#0	Reservation	Physical_ID	Request_channel_number	Request_bw
	7	6	6	13
	start_second_count_hi			start_second_count_lo
#1	Reservation	Physical_ID	Request_channel_number	Request_bw
	7	6	6	13
	start_second_count_hi			start_second_count_lo
#2	Reservation	Physical_ID	Request_channel_number	Request_bw
	7	6	6	13
	start_second_count_hi			start_second_count_lo
#M	Reservation	Physical_ID	Request_channel_number	Request_bw
	7	6	6	13
	start_second_count_hi			start_second_count_lo

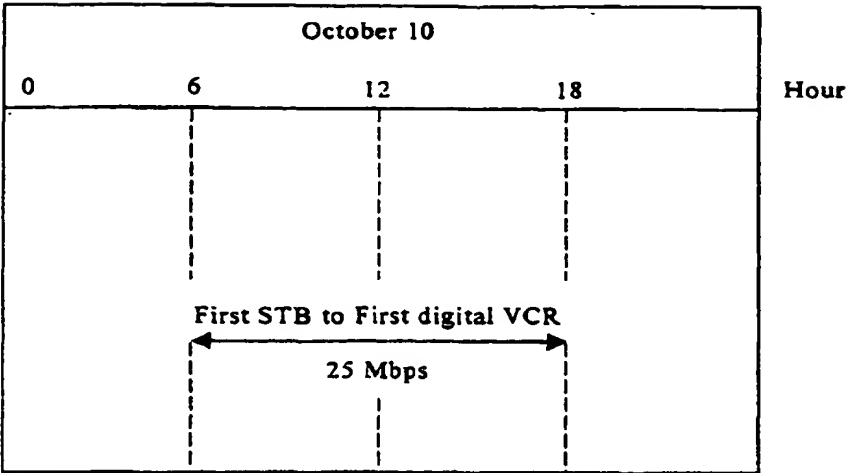
## Initial value

Reservation	XXXXXX	XXXXXX	000000000000
7	6	6	13
XXXXXXXXXXXXXXXXXXXXXXXXXXXX			XXXXXX
25			7
XXXXXXXXXXXXXXXXXXXXXXXXXXXX			XXXXXX

Fig. 2

*Fig. 3*

(a)



(b)

#0	Reservation	000000	000001	0011000100000
	7	6	6	13
	0000000000000000010101000			1100000
#1	Reservation	xxxxxxx	xxxxxxx	0000000000000
	7	6	6	13
	xxxxxxxxxxxxxxxxxxxxxxxxxxxx			xxxxxxxxx
#2	Reservation	xxxxxxx	xxxxxxx	0000000000000
	7	6	6	13
	xxxxxxxxxxxxxxxxxxxxxxxxxxxx			xxxxxxxxx

Fig. 4

October 10 0 o'clock   6 o'clock	BANDWIDTH_AVAILABLE bw_remaining	1001100110011
	channel_available_lo	1111111111111111 1111111111111111
October 10 6 o'clock   18 o'clock	BANDWIDTH_AVAILABLE bw_remaining	0110100010011
	channel_available_lo	1111111111111111 1111111111111101
October 10 18 o'clock   24 o'clock	BANDWIDTH_AVAILABLE bw_remaining	1001100110011
	channel_available_lo	1111111111111111 1111111111111111

Fig. 5

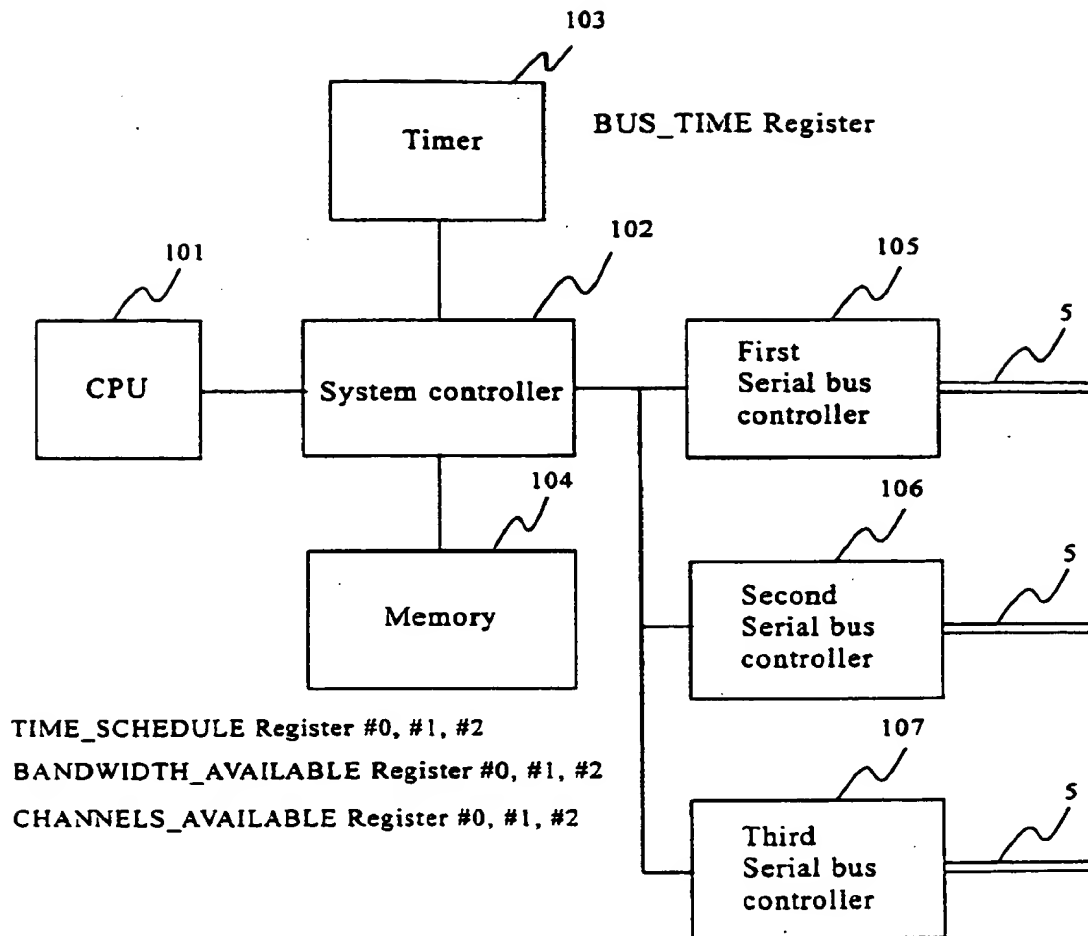


Fig. 6

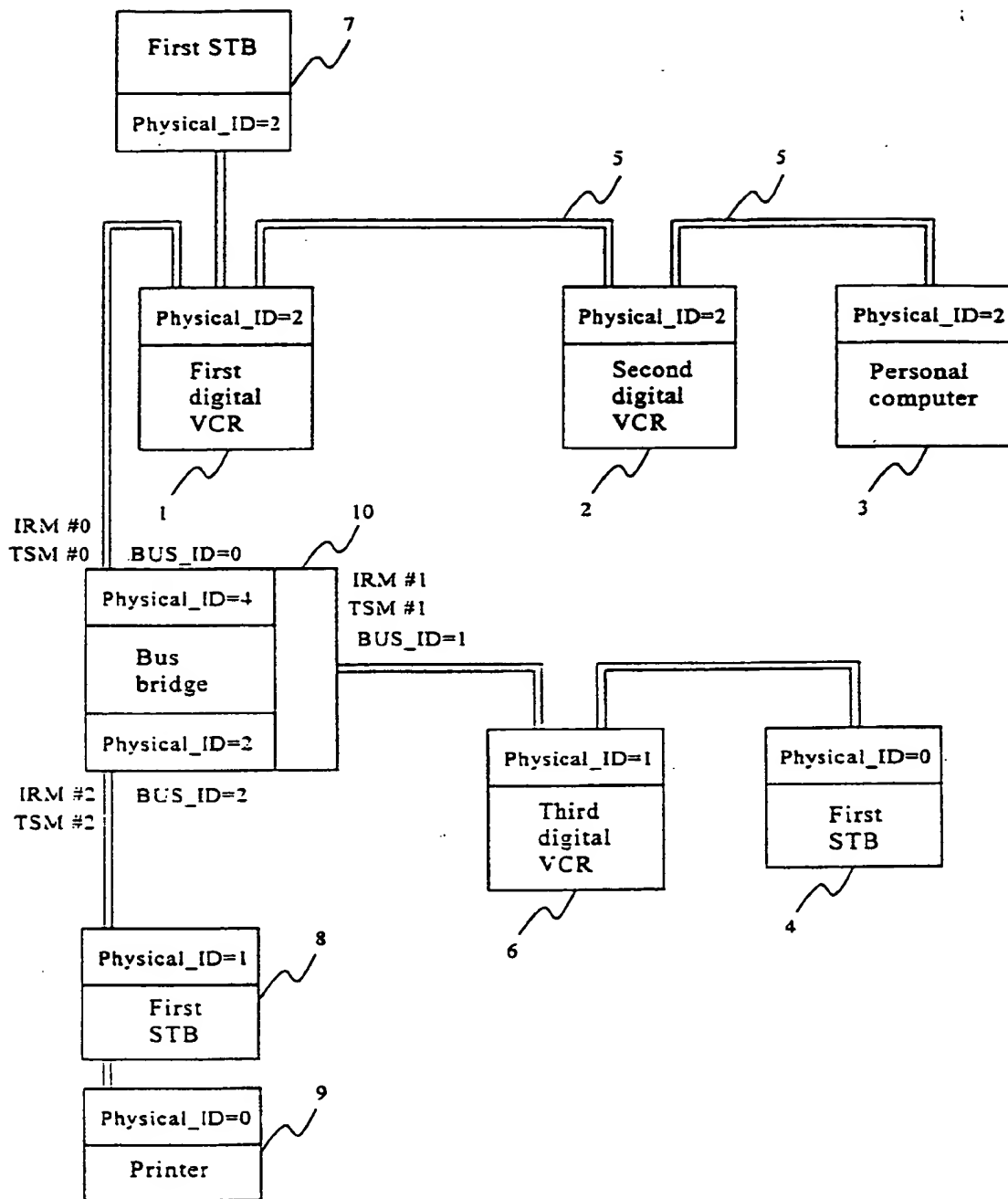


Fig. 7



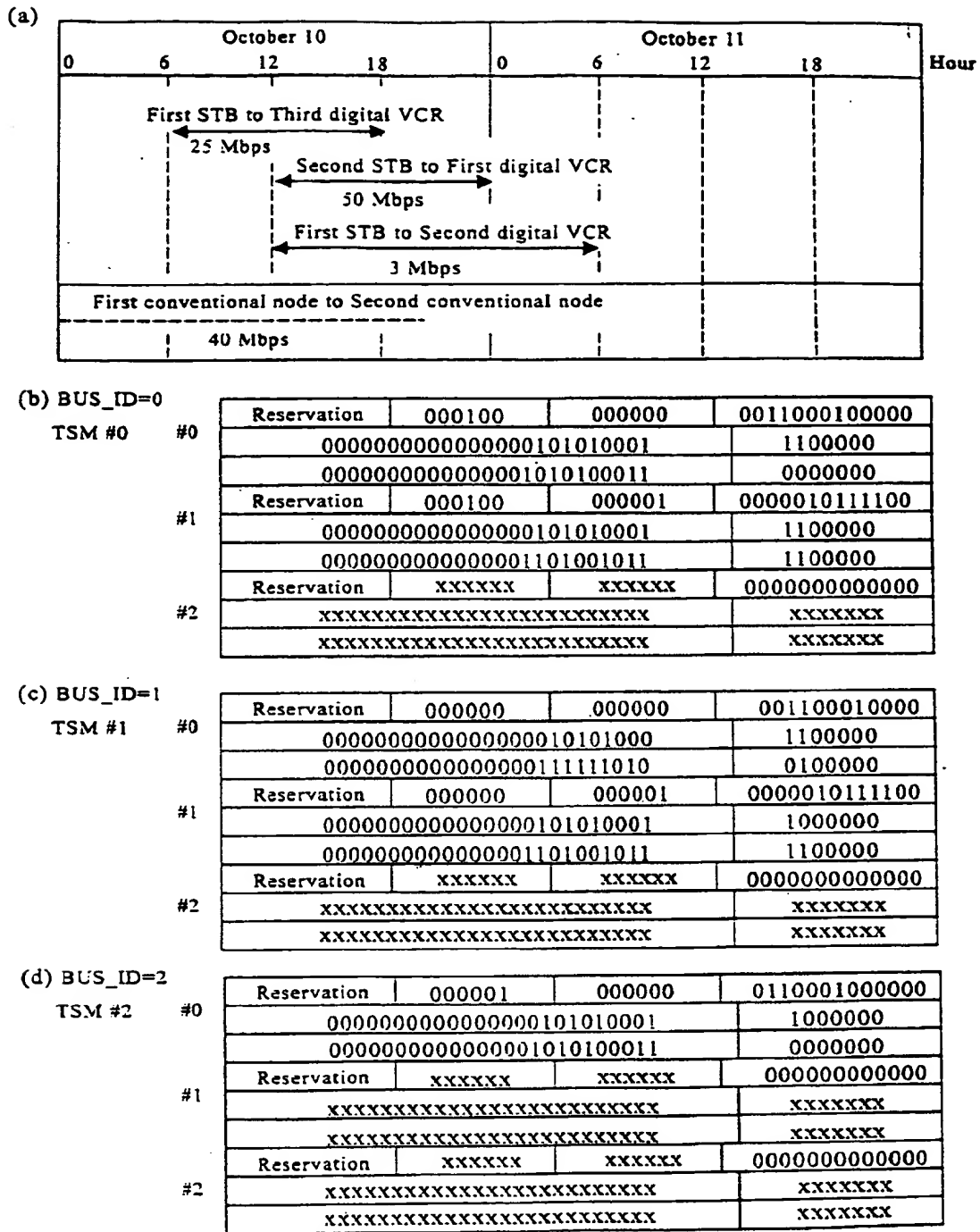


Fig. 8

[illegible]

Fig. 9

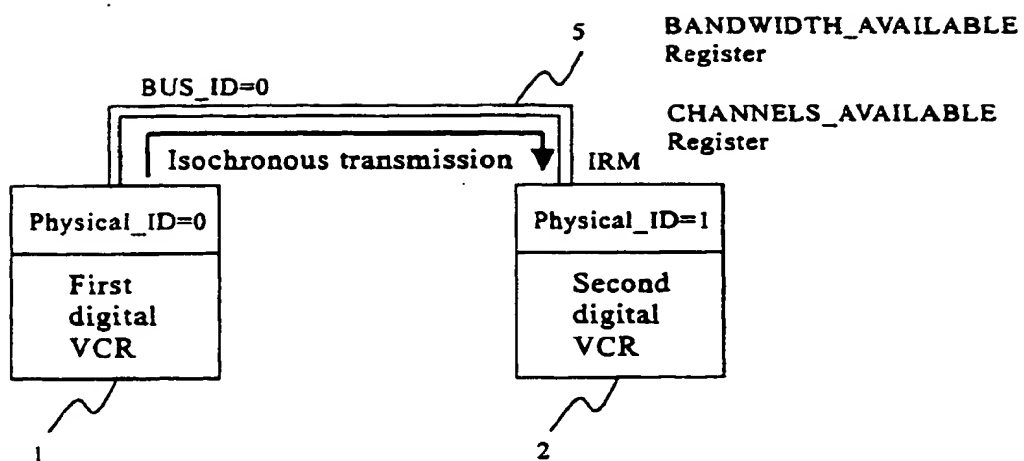


Fig. 10

Definition

Reservation	bw_remaining
19	13

Initial value

00000000000000000000	1001100110011
----------------------	---------------

BANDWIDTH\_AVAILABLE Register

*Fig. 11*

Definition

channels_available_hi
32
channels_available_lo
32

Initial value

32
32

CHANNELS\_AVAILABLE Register

Fig. 12

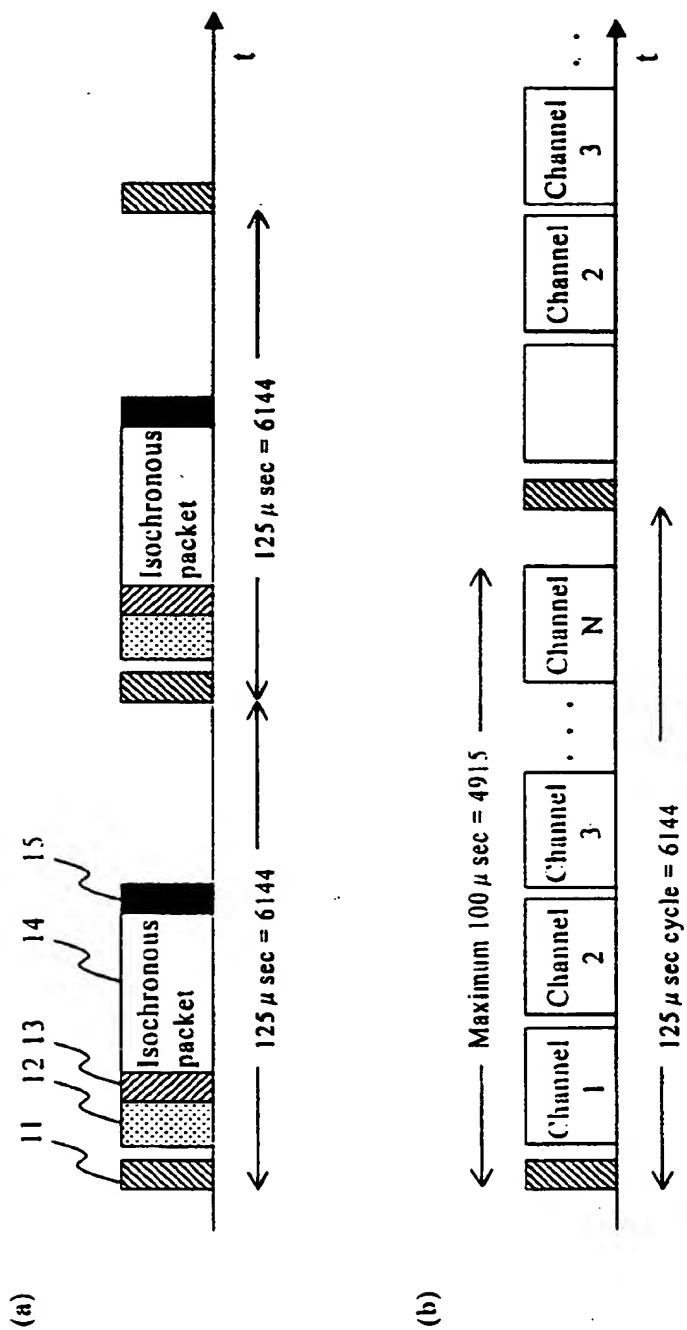


Fig. 13

Definition

second_count_hi	second_count_lo
25	7

BUS\_TIME Register

*Fig. 14*

Definition

BUS_ID	Physical_ID	Request_channel _number	Request_bw
start_second_count_hi			start_second_count_lo
end_second_count_hi			end_second_count_lo

TIME\_SCHEDULE Register

*Fig. 15*